Electronic Version
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Claims

[c1] 1. A pipeline-based circuit comprising:
a plurality of processing units cascaded to establish at least a pipeline, each processing unit comprising:
a logic unit for performing a predetermined logic operation;
a first buffer unit electrically connected to the logic unit for piping an output data of the logic unit to a logic unit of a next processing unit according to a clock signal, the clock signal cyclically transitioning between a first logic value and a second logic value;
a clock-gating unit electrically connected to the first buffer unit for determining if the clock signal inputted into the first buffer unit is gated according to a control value for making the clock signal correspond to the first logic value when the processing unit starts working; and
a second buffer unit electrically connected to the clock-gating unit for storing the control value;
a pipeline control unit for generating at least a control signal to each processing unit for controlling if an output data associated with a processing unit is piped to a next processing unit; and
a control value generator for setting the control value of

each processing unit according to a plurality of control signals outputted from the pipeline control unit.

[c2] 2. The pipeline-based circuit of claim 1 wherein the first logic value is "0", and the second logic value is "1".

[c3] 3. The pipeline-based circuit of claim 1 wherein the first buffer unit comprises at least a flip-flop.

[c4] 4. The pipeline-based circuit of claim 1 wherein the second buffer unit comprises at least a flip-flop.

[c5] 5. The pipeline-based circuit of claim 1 wherein the pipeline control unit is capable of generating a first control signal to each processing unit for piping the output data of the logic unit to the next processing unit, and is capable of generating a second control signal to each processing unit for nullifying the output data of the logic unit.

[c6] 6. The pipeline-based circuit of claim 5 wherein when a control value of a first processing unit holds a predetermined value for controlling a clock-gating of the first processing unit not to gate the clock signal, the pipeline control unit does not output the first control signal to a processing unit before the first processing unit, the pipeline control unit does not output the first control signal to the first processing unit, and the pipeline con-

trol unit does not output the second control signal to the first processing unit, the control value of the first processing unit is capable of maintaining the predetermined value.

[c7] 7. The pipeline-based circuit of claim 5 wherein when the pipeline control unit outputs the first control signal and the second control signal to a first processing unit, a control value of a processing unit following the first processing unit is capable of being set to a predetermined value for driving a clock-gating unit of the processing unit following the first processing unit to gate the clock signal.

[c8] 8. The pipeline-based circuit of claim 5 wherein when the pipeline control unit outputs the first control signal to a first processing unit, and the pipeline control unit does not output the first control signal to a processing unit before the first processing unit, a control value of the first processing unit is capable of being set to a predetermined value for driving a clock-gating unit of the first processing unit to gate the clock signal.

[c9] 9. The pipeline-based circuit of claim 5 wherein when a control value of a first processing unit holds a predetermined value for driving a clock-gating unit of the first processing unit to gate the clock signal, and the pipeline

control unit outputs the first control signal to the first processing unit, a control value of a processing unit following the first processing unit is capable of being set to the predetermined value.

[c10] 10. The pipeline-based circuit of claim 1 being built according to a super-scalar structure.

[c11] 11. The pipeline-based circuit of claim 1 being built according to a super-pipeline structure.

[c12] 12. The pipeline-based circuit of claim 1 being a microprocessor.

[c13] 13. The pipeline-based circuit of claim 1 being a digital signal processor (DSP).

[c14] 14. A method of controlling a clock signal for a pipeline-based circuit, the pipeline-based circuit comprising:
a plurality of processing units cascaded to establish at least a pipeline, each processing unit comprising:
a logic unit for performing a predetermined logic operation; and
a first buffer unit electrically connected to the logic unit for piping an output data of the logic unit to a logic unit of a next processing unit according to a clock signal, the clock signal cyclically transitioning between a first logic value and a second logic value; the method comprising:

installing a clock-gating unit in each processing unit and connecting the clock-gating unit and the first buffer unit for gating the clock signal inputted into the first buffer unit to make the clock signal correspond to the first logic value;

installing a second buffer unit in each processing unit and connecting the second buffer unit and the clock-gating unit for storing the control value;

installing a pipeline control unit for generating at least a control signal to each processing unit to control if an output data associated with a processing unit is piped to a next processing unit;

utilizing a plurality of control signals generated from the pipeline control to set the control value of each processing unit; and

utilizing the control value of each processing unit to control if the corresponding clock-gating unit gates the clock signal inputted into the corresponding first buffer unit when each processing unit starts working.

[c15] 15. The method of claim 14 wherein the first logic value is "0", and the second logic value is "1".

[c16] 16. The method of claim 14 wherein the first buffer unit comprises at least a flip-flop.

[c17] 17. The method of claim 14 wherein the second buffer

unit comprises at least a flip-flop.

[c18] 18. The method of claim 14 wherein when the pipeline control unit generates a first control signal to each processing unit, the output data of the logic unit is piped to the next processing unit, and when the pipeline control unit generates a second control signal to each processing unit, the output data of the logic unit is nullified.

[c19] 19. The method of claim 18 wherein the step of setting the control value of each processing unit comprises: when a control value of a first processing unit holds a predetermined value for controlling a clock-gating of the first processing unit not to gate the clock signal, the pipeline control unit does not output the first control signal to a processing unit before the first processing unit, the pipeline control unit does not output the first control signal to the first processing unit, and the pipeline control unit does not output the second control signal to the first processing unit, the control value of the first processing unit maintains the predetermined value.

[c20] 20. The method of claim 18 wherein the step of setting the control value of each processing unit comprises: when the pipeline control unit outputs the first control signal and the second control signal to a first processing

unit, a control value of a processing unit following the first processing unit is set to a predetermined value for driving a clock-gating unit of the processing unit following the first processing unit to gate the clock signal.

[c21] 21. The method of claim 18 wherein the step of setting the control value of each processing unit comprises: when the pipeline control unit outputs the first control signal to a first processing unit, and the pipeline control unit does not output the first control signal to a processing unit before the first processing unit, a control value of the first processing unit is set to a predetermined value for driving a clock-gating unit of the first processing unit to gate the clock signal.

[c22] 22. The method of claim 18 wherein the step of setting the control value of each processing unit comprises: when a control value of a first processing unit holds a predetermined value for driving a clock-gating unit of the first processing unit to gate the clock signal, and the pipeline control unit outputs the first control signal to the first processing unit, a control value of a processing unit following the first processing unit is set to the predetermined value.

[c23] 23. The method of claim 18 wherein the step of setting the control value of each processing unit comprises:

when a control value of a first processing unit holds a predetermined value for controlling a clock-gating of the first processing unit not to gate the clock signal, the pipeline control unit outputs the first control signal to the first processing unit, the pipeline control unit does not output the second control signal to the first processing unit, a control value of a processing unit following the first processing unit is set to the predetermined value.

[c24] 24. The method of claim 14 wherein the pipeline-based circuit is built according to a super-scalar structure.

[c25] 25. The method of claim 14 wherein the pipeline-based circuit is built according to a super-pipeline structure.

[c26] 26. The method of claim 14 wherein the pipeline-based circuit is a microprocessor.

[c27] 27. The method of claim 14 wherein the pipeline-based circuit is a digital signal processor (DSP).